Project Introduction

We will develop an efficient Graphics Processing Unit (GPU) based parallel Binary Decision Diagram (BDD) software package, and will also combine it with our GPU-based parallel SAT solver that we are currently developing in a NASA SBIR Phase II project in order to solve much larger and more complex Boolean formulas from formal verification than possible with either method alone. BDDs are a data structure that satisfies some simple restrictions, resulting in a unique representation of a Boolean function regardless of its actual implementation. This property of BDDs allows the efficient solution of many problems. The proposed tool will exploit multi-core CPUs and the thousands of stream cores in the latest GPUs, which were made accessible to programmers through specialized software development kits. These large numbers of stream cores in GPUs, and the possibility to execute non-graphics computations on them, open unprecedented levels of parallelism at a very low cost. In the last 8 years, GPUs had an increasing performance advantage of an order of magnitude relative to x86 CPUs. Furthermore, this performance advantage will continue to increase in the next 20 years because of the scalability of the chip manufacturing processes. The technical objectives will be to efficiently exploit the GPU parallelism in order to accelerate the execution of our prototype GPU-based parallel BDD package, and to implement hybrid approaches combining it with our GPU-based parallel SAT solver. BDDs and SAT solvers are orthogonal methods with different advantages, and a hybrid of the two will significantly increase both the speed and capacity when formally verifying complex software for space missions. We achieved at least 2 orders of magnitude speedup with our prototype GPU-based parallel BDD package in a previous Phase I, and expect to achieve at least 4 orders of magnitude speedup with our hybrid BDD-SAT tool by the end of Phase II, compared to the current state of the art.
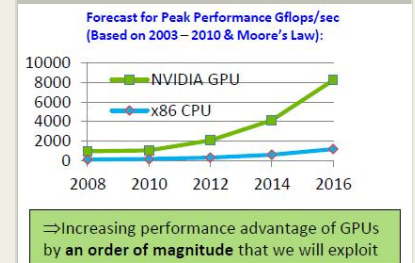
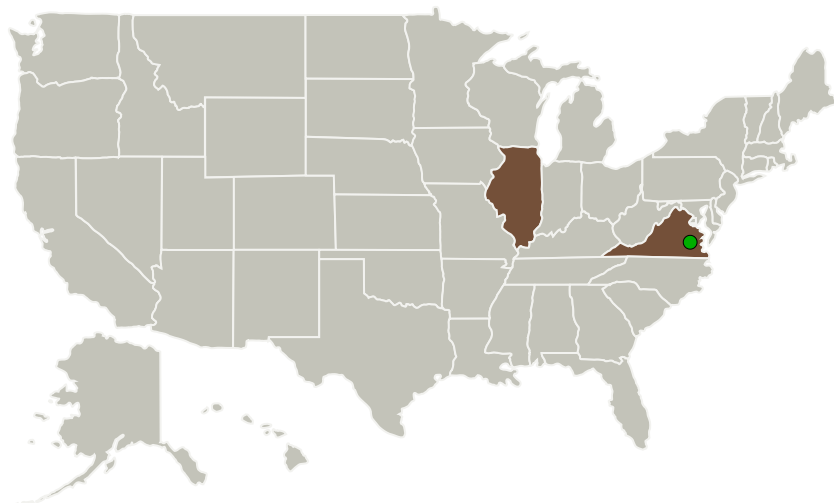Scalable Parallel Algorithms for Formal Verification of Software

Table of Contents

Primary U.S. Work Locations and Key Partners

Organizations Performing Work	Role	Type	Location
Aries Design Automation, LLC	Lead Organization	Industry	Chicago, Illinois
●Langley Research Center(LaRC)	Supporting Organization	NASA Center	Hampton, Virginia

Primary U.S. Work Locations	
Illinois	Virginia

Project Transitions

▶ **May 2013:** Project Start

✓ **November 2013:** Closed out

Closeout Documentation:
- Final Summary Chart(*https://techport.nasa.gov/file/139910*)

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Organization:

Aries Design Automation, LLC

Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

Project Management

Program Director:

Jason L Kessler

Program Manager:

Carlos Torrez

Principal Investigator:
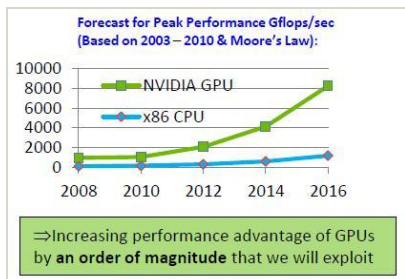
Miroslav N Velev

Co-Investigator:

Miroslav Velev

Images

Project Image
Scalable Parallel Algorithms for
Formal Verification of Software
*(https://techport.nasa.gov/imag
e/129987)*

Technology Maturity (TRL)

Start: **3**
Current: **4**
Estimated End: **4**

1	2	3	4	5	6	7	8	9
Applied Research			Development			Demo & Test		
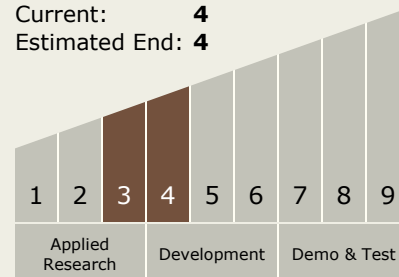
Technology Areas

Primary:

- TX11 Software, Modeling, Simulation, and Information Processing
  └ TX11.1 Software Development, Engineering, and Integrity
    └ TX11.1.8 Software Analysis and Design Tools

Target Destinations

The Sun, Earth, The Moon, Mars, Others Inside the Solar System, Outside the Solar System

Tech Port

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For more information and an accessible alternative, please visit:
https://techport.nasa.gov/view/12869

Page 3